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10/577,863	04/28/2006	Masamichi Ishihara	OKI.979	2248

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EXAMINER	
HARRISTON, WILLIAM A	
ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
03/18/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/577,863	ISHIHARA, MASAMICHI	
	Examiner	Art Unit	
	WILLIAM HARRISTON	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 47-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 47-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/5/2007, 4/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/26/2010 has been entered.

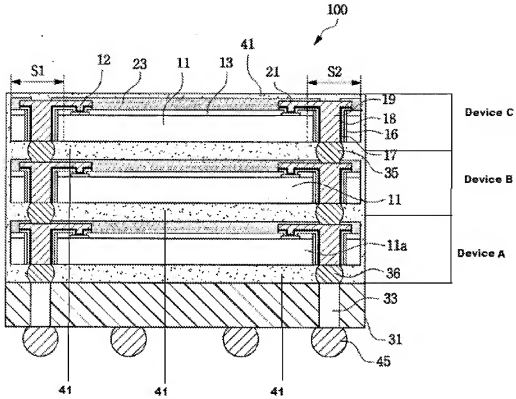
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 10-23 and 47-51 are rejected under 35 U.S.C. 102 (b) as being anticipated by Lee et al. (US 20050046002 hereafter Lee).

3. Examiner's note: To easily identify which common elements belong to which semiconductor device the Examiner has designated elements belonging to the first, second and third semiconductor devices with a, c, and b respectively.



4. Regarding claim 1, Lee discloses a stacked semiconductor device consisting of a first semiconductor device (Device A in annotated figure 3) having outside electrode terminals (36 in figure 3) on a lower surface thereof, a second semiconductor device (Device C in annotated figure 3) electrically connected with said first semiconductor device (See paragraph 0028 lines 1-3) and secured on said first semiconductor device, said first semiconductor device (Device A) comprising:

a first semiconductor substrate (11a in figure 3);

first circuit elements (12a in figure 3, see paragraph 0027 line 14) at a first main surface of said first semiconductor substrate;

a first multilayer wiring part (21a and 23a in figure 3) on said first circuit elements (12a in figure 3) and configured of a first wiring (21a in figure 3) electrically connected with said first circuit elements (12a in figure 3, see paragraph 0027 lines 13-15) and a first insulating material layer (23a in figure 3), the first wiring (21a in figure 3) and the first insulating material layer (23a in figure 3) being stacked alternately with the first insulating material layer being an uppermost layer;

a first insulating layer (41 between Device A and Device B in annotated figure 3) for covering said first insulating material layer (23a in figure 3) of said first multilayer wiring part and provided over the first main surface of said first semiconductor substrate, said first insulating layer (41 in figure 3) is a support member of said first semiconductor substrate;

a second insulating layer (41 between element 31 and Device A) for covering a second main surface of said first semiconductor substrate (11a in figure 3) that is opposite the first main surface of said first semiconductor substrate;

a plurality of first post electrodes (35 in figure 3) on said first wiring (21a in figure 3) of said first multilayer wiring part and each having a top surface and side surfaces, the top surfaces of said first post electrodes exposed from a surface of said first insulating layer (41 between Device A and Device B in figure 3) and all the side surfaces of said first post electrodes covered by said first insulating layer;

a plurality of first through-type electrodes (19a in figure 3) penetrating from a specified depth of said first multilayer wiring part (21a in figure 3) to a surface of said second insulating layer (41 between element 31 and Device A in figure 3) through said

first semiconductor substrate (11a in figure 3), said first through-type electrodes insulated from said first semiconductor substrate by a first insulating film (16 in figure 3, see paragraph 0037 lines 1-8) and connected with said first wiring (21a in figure 3) of said first multilayer wiring part; and

said outside electrode terminals (36 in figure 3) connected to said first through-type electrodes (19a in figure 3),

said second semiconductor device (Device C in figure 3) comprising:

a second semiconductor substrate (11c in figure 3);

second circuit elements (12c in figure 3) formed at a first main surface of said second semiconductor substrate;

a second multilayer wiring part (21c and 23c in figure 3) on said second plurality of circuit elements (12c in figure 3) and configured of a second wiring (21c in figure 3) electrically connected with said second circuit elements (see paragraph 0027 lines 13-15) and a second insulating material layer (23c in figure 3), the second wiring and the second insulating material layer being stacked alternately with the second insulating material layer being an uppermost layer;

a third insulating layer (41 above Device C in figure 3) for covering said second insulating material layer (23c in figure 3) of said second multilayer wiring part and provided over the first main surface of said second semiconductor substrate, said third insulating layer (41 above Device C in figure 3) is a support member of said second semiconductor substrate;

a fourth insulating layer (41 between Device C and Device B in figure 3) for

covering a second main surface of said second semiconductor substrate that is opposite the first main surface of said second semiconductor substrate; and

a plurality of second through-type electrodes (19c in figure 3) penetrating from a specified depth of said second multilayer wiring part to a surface of said fourth insulating layer (41 Between Device B and Device C in figure 3) provided to pierce through said second semiconductor substrate (11c in figure 3), said second through-type electrodes insulated from said second semiconductor substrate by a second insulating film (16c in figure 3, see paragraph 0037 lines 1-8) and connected with said second wiring (21c in figure 3) of said second multilayer wiring part,

in said first semiconductor device (Device A), said first through-type electrodes (19a in figure 3) are at the lower surface thereof and are provided with said outside electrode terminals (36 in figure 3), and

said second post electrodes (35 in figure 3) at a lower surface of said second semiconductor device (Device C) are electrically connected with said first post electrodes (35 in figure 3) at an upper surface of said first semiconductor device through joints.

Examiner has interpreted a joint to be a location where two elements make contact.

5. Regarding claim 2, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

a third semiconductor device (Device B in figure 3) stacked and secured between said first semiconductor device (Device A) and said second semiconductor device

(Device C), wherein said third semiconductor device comprises:

a third semiconductor substrate (11b in figure 3);

third circuit elements (12b in figure 3) at a first main surface of said third semiconductor substrate;

a third multilayer wiring part (21b and 23b in figure 3) on said third circuit elements and configured of a third wiring (21b in figure 3) electrically connected with said third circuit elements (see paragraph 0027 lines 11-13) and a third insulating material layer (23b in figure 3), the third wiring and the third insulating material layer being stacked alternately with the third insulating material layer being an uppermost layer;

a fifth insulating layer (41 between Device B and Device C in figure 3) for covering said third insulating material layer (23b in figure 3) of said third multilayer wiring part and provided over the first main surface of said third semiconductor substrate, said fifth insulating layer is a support member of said third semiconductor substrate;

a sixth insulating layer (41 between device A and Device B in figure 3) for covering a second main surface of said third semiconductor substrate that is opposite the first main surface of said third semiconductor substrate;

a plurality of third post electrodes (35 in figure 3) on said third wiring (21b in figure 3) of said third multilayer wiring part and each having a top surface and side surfaces, the top surfaces of said third post electrodes exposed from a surface of said fifth insulating layer and all the side surfaces of said third post electrodes covered

by said fifth insulating layer;

a plurality of third through-type electrodes (19b in figure 3) penetrating from a specified depth of said third multi-layer wiring part to a surface of said sixth insulating layer through said third semiconductor substrate said third through-type electrodes (19b in figure 3) insulated from said third semiconductor substrate by a third insulating film (16b in figure 3, see paragraph 0037 lines 1-8) and connected with said third wiring of said third multilayer wiring part,-and

the third through-type electrodes (19b in figure 3) on upper/lower surfaces of said third semiconductor device are electrically connected with the first through-type electrodes (19a in figure 3) of the first semiconductor device at an upper stage side and the second semiconductor device (11c in figure 3) at a lower stage side through joints (see paragraph 28 lines 1-3).

6. Regarding claim 3, Lee discloses the device of claim1 for the reasons stated above. Lee further discloses:

wherein said first and second semiconductor devices (11a and 11c in figure 3) are disposed as a single body, have a same size, and overlap each other. See paragraph 0032.

7. Regarding claim 4, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein a plurality of said second semiconductor devices that are smaller than said first semiconductor device, and are disposed and secured in parallel on said first

semiconductor device. Lee discloses the chips may have different sizes, see Paragraph 0032.

Lee discloses the devices are electrically interconnected. One having skill in the art would understand this to mean the devices share a common voltage. A parallel connection is established when electronic components have the same voltage across their ends.

8. Regarding claim 5, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein first through-type electrodes (19a in figure 3) and the second through-type electrodes (19c in figure 3) are brought into correspondence and are electrically connected respectively through said joints.

9. Regarding claim 6, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein said joints comprise metal joining.

Examiner has interpreted joining to occur when two elements make contact with each other.

10. Regarding claim 7, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein said first and second post electrodes (35 in figure 3) comprise stud bump electrodes.

11. Regarding claim 11, Lee discloses the device of claim 1 for the reasons stated above: Lee further discloses:

wherein said first and second through-type electrodes (19a and 19c in figure 3) and said first and second post electrodes (35 and 36 in figure 3) comprise copper, tungsten, titanium, nickel, aluminum or an alloy thereof. See paragraph 0030 lines 9-12 and 0037 lines 16-19.

12. Regarding claim 12, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein a gap between said first semiconductor device (Device A) and said second semiconductor device (Device C) is filled with an insulating resin (41 in figure 3). See paragraph 0049 lines 1-3.

13. Regarding claim 13, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein said first and second semiconductor devices (11a and 11c in figure 3) respectively have the first and second post electrodes (35 in figure 3) exposed in surfaces of said first and third insulating layers (41 in figure 3), and said first and second through-type electrodes (19a and 19c in figure 3) exposed in surfaces, of said second and fourth insulating layers (41 in figure 3), and said first and second through-type electrodes are formed at exposed ends of specified ones of said first and second post electrodes or said first and second through-type electrodes located in an upper surface.

14. Regarding claim 14, Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein said first and second post electrodes (35 in figure 3) have larger diameter than said first and second through-type electrodes (19a and 19c in figure 3).

15. Regarding claim 15 Lee discloses the device of claim 1 for the reasons stated above. Lee further discloses:

wherein said first and second circuit elements (12a and 12c in figure 3) are passive elements.

16. Regarding claim 16, Lee discloses the device of claim 1 for the reasons stated above, Lee further discloses:

wherein said first and second semiconductor substrates have a thickness of around 5 to 50 micrometers and said first and third insulating layers have a thickness of around 20 to 100 pm.

Lee suggests thinning the semiconductor substrate to a thickness of 50 micrometers or less before stacking. See paragraph 0039 lines 8-11.

Regarding the thickness of the insulating layers 41, Lee discloses post electrodes 35 have a diameter of 20-60 micrometers. Lee further discloses the top surface of the post electrodes are exposed by an opening at a surface of the insulating layer. See paragraph 0030 lines 9-10. One having skill in the art would understand the diameter of the post electrodes 35 is greater than or equal to the height of layer 41, therefore satisfying the claimed structural limitations.

17. Regarding claim 17, Lee discloses a semiconductor device comprising:

a semiconductor substrate (11 in figure 3);

circuit elements (12 in figure 3) at a first main surface side of said semiconductor substrate;

a multilayer wiring part (21 and 23 in figure 3) on said circuit elements and configured of a wiring (21 in figure 3) electrically connected with said circuit elements and an insulating layer (23 in figure 3 of Lee), the wiring and the insulating layer being stacked alternately with the insulating layer being an uppermost layer;

a first insulating layer (41 in figure 3) for covering said insulating layer (23 in figure 3) of said multilayer wiring part and provided over the first main surface of said semiconductor substrate, said first insulating layer is a support member of said semiconductor substrate;

a second insulating layer (41 in figure 3) for covering a second main surface of said semiconductor substrate that is opposite the first main surface;

a plurality of post electrodes (35 in figure 3) formed on said wiring (21 in figure 3) of said multilayer wiring part and each having a top surface and side surfaces, the top surfaces exposed from a surface of said first insulating layer (41 in figure 3) and all the side surfaces covered by said first insulating layer; and

a plurality of through-type electrodes (19 in figure 3) penetrating from a specified depth of said multilayer wiring part to a surface of said second insulating layer provided to pierce through said semiconductor substrate, said through-type electrodes insulated

from said semiconductor substrate by an insulating film (16 in figure 3) and connected with said wiring (21 in figure 3) of said multilayer wiring part.

18. Regarding claim 18, Lee discloses the device of claim 17 for the reasons stated above. Lee further discloses:

protruding electrodes (45 in figure 3) at exposed ends of specified ones of said post electrodes (35 and 36 in figure 3) and said through-type electrodes (19 in figure 3).

19. Regarding claim 19, Lee discloses the device of claim 17 for the reasons stated above. Lee further discloses:

wherein said post electrodes (35 in figure 3) have larger diameter than said through-type electrodes (19 in figure 3).

20. Regarding claim 20, Lee discloses the device of claim 17 for the reasons stated above. Lee further discloses:

wherein said post electrodes (35 and 36 in figure 3) are comprised of stud bump electrodes.

21. Regarding claim 21, Lee discloses the device of claim 17 for the reasons stated above. Lee further discloses:

wherein said through-type electrodes (19 in figure 3) and said post electrodes (35 in figure 3) comprise copper, tungsten, titanium, nickel, aluminum or an alloy thereof. See paragraph 0030 lines 9-12 and 0037 lines 16-19.

22. Regarding claim 22, Lee discloses the device of claim 17 for the reasons stated above. Lee further discloses:

wherein said circuit elements (12 in figure 3) are passive elements.

23. Regarding claim 23, Lee discloses the device of claim 17 for the reasons stated above. Lee further discloses:

wherein said semiconductor substrate has a thickness of around 5 to 50 micrometers and said first insulating layer (41 in figure 3) has thickness of around 20 to 100 pm.

Lee suggests thinning the semiconductor substrate to a thickness of 50 micrometers or less. See paragraph 0039 lines 8-11.

Regarding the thickness of the insulating layers 41, Lee discloses post electrodes 35 have a diameter of 20-60 micrometers. Lee further discloses the top surface of the post electrodes are exposed by an opening at a surface of the insulating layer. See paragraph 0030 lines 9-10. One having skill in the art would understand the diameter of the post electrodes 35 is equal to or greater than the height of the layer 41, therefore satisfying the claimed structural limitations.

24. Regard in claim 47, Lee discloses a semiconductor device comprising:

a semiconductor substrate (11 in figure 3) having first and second main surfaces, and a circuit (underneath of passivation layer 13 in figure 3, see paragraph 0034 lines 6-8) on the first main surface;

a multilayer wiring part (21 and 23 in figure 3) including an insulating layer (23 in

figure 3) and a wiring pattern (21 in figure 3) electrically connected with the circuit (via chip pads 12 in figure 3), the insulating layer and the wiring pattern disposed over the first main surface alternately with respect to each other;

a first insulating layer (41 in figure 3) on an uppermost layer of said multilayer wiring part (23 in figure 3) over the first main surface of said semiconductor substrate, said first insulating layer is a support member of said semiconductor substrate;

a second insulating layer (41 in figure 3) over the second main surface;

a first electrode (35 in figure 3) over the first main surface, the first electrode having top and side surfaces and electrically connected with a part of the wiring pattern (21 in figure 3), the top surface being exposed from a surface of said first insulating layer (41 in figure 3) and all the side surfaces being covered with said first insulating layer; and

a second electrode (19 in figure 3) formed on an inner wall of a through-via which penetrates from the first main surface to the second main surface.

25. Regarding claim 48, Lee discloses the device of claim 47 for the reasons stated above. Lee further discloses:

wherein said first insulating layer (41 in figure 3) is thicker than the insulating layer (23 in figure 3) of said multilayer wiring part.

26. Regarding claim 49, Lee discloses the device of claim 47 for the reasons stated above. Lee further discloses:

wherein said first insulating layer (41 in figure 3) is thicker than said semiconductor substrate (11 in figure 3).

27. Regarding claim 50, Lee discloses the device of claim 47 for the reasons stated above. Lee further discloses:

wherein said first insulating layer (41 in figure 3) comprises encapsulation resin. See paragraph 0049 lines 1-3.

28. Regarding claim 51,Lee discloses the device of claim 47 for the reasons stated above. Lee further discloses:

wherein said second electrode (19 in figure 3) is a through-type electrode.

Claim Rejections - 35 USC § 103

29. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

30. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

31. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Murata et al. (US 20020030266).

32. Regarding claim 8, Lee discloses the device of claim 1 for the reasons stated above. Lee does not disclose metal plate having insulating holes.

However, of Murata does disclose a metal plate (10a in figure 1c) having insulating holes (18 in figure 1c).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Murata with the teachings of Lee in order to improve the performance of a stacked device by ensuring adequate flatness and providing heat dispersion between adjacent devices.

Further, Lee suggests an interposer (i.e. a metal plate) may be incorporated into the chip stack. See paragraph 0031.

Further, Lee in view of Murata disclose wherein in a portion of said insulating holes, first ones of said first post electrodes (35 in figure 3 of Lee) at an upper surface of said first semiconductor device (11a in figure 3 of Lee) are electrically connected with first ones of said second through- type electrodes at a lower surface of said second semiconductor device(11c in figure 3 of Lee) through said joints in a state without contacting said metal plate, and second ones of said first through-type electrodes and said first post electrodes of said first semiconductor device and second ones of said second through-type electrodes and said second post electrodes of said second semiconductor device that face said metal plate are electrically connected with said metal pate through said joints.

33. Regarding claim 9, Lee in view of Murata disclose the device of claim 1 for the reasons sated above. However, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Conclusion

34. Applicant is advised that the argued intended use of the insulating layer, i.e. "supporting a semiconductor substrate" does not constitute a structural difference between the claimed invention and the prior art.

Further, the method of making a device, i.e. polishing a second main surface of a semiconductor substrate, is not germane to the patentability of the device itself.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM HARRISTON whose telephone number is (571)270-3897. The examiner can normally be reached on Monday - Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. H./
Examiner, Art Unit 2826
3/3/2010

/Leonardo Andújar/
Primary Examiner, Art Unit 2826